

CLAIMS

What is claimed is:

1 1. An apparatus comprising:

2 a circular shift register having N data samples to circularly shift a first data
3 sample of the N data samples into a data position at a first clock frequency, the N
4 data samples corresponding to signal received from one of K satellites in a global
5 positioning system (GPS), the N data samples being loaded into the circular shift
6 register at a second clock frequency; *K, N define*

7 K storage elements to store K code sequences, respectively, each of the K
8 code sequences having N code samples and including a first code sample being
9 written at a code position corresponding to the data position at a third clock
10 frequency, the K storage elements corresponding to the K satellites; and

11 a code register to store the N code samples loaded from one of the K
12 storage elements at a fourth clock frequency, the fourth clock frequency being K
13 times faster than the first clock frequency.

1 2. The apparatus of claim 1 further comprising:

2 a write circuit coupled to the K storage elements to write the K first code
3 samples to the K storage elements, respectively, at the K code positions
4 synchronously with the shifted first data sample.

1 3. The apparatus of claim 1 further comprising:
2 a correlator circuit coupled to the circular shift register and the code
3 register to compute a correlation result from the N data samples and the N code
4 samples.

1 4. The apparatus of claim 1 wherein each of the K storage elements is
2 one of a plurality of flip-flops, a register, a row in a random access memory
3 (RAM).

1 5. The apparatus of claim 2 wherein the write circuit comprises:
2 a plurality of decoders coupled to the K storage elements to enable writing
3 the K first code samples to the K code positions synchronously with the shifted
4 first data sample.

6. The apparatus of claim 3 wherein the correlator circuit comprises:

- a mapper to map the N data samples and the corresponding N code samples into a plurality of mapper out puts; [?]
splitting
- an adder to add the plurality of mapper outputs to generate a result sum;
- and
- a subtractor to subtract a bias value from the result sum to generate the correlation result.

1 7. The apparatus of claim 6 wherein each of the N code samples is a
2 pseudo random noise (PN) code being represented by a one-bit value.

1 8. The apparatus of claim 7 wherein each of the N data samples is a
2 two-bit with value of one of 01, 10, and 11.

1 9. The apparatus of claim 8 wherein each of the mapper outputs is
2 two-bit with value of one of 01, 10, and 11.

1 10. The apparatus of claim 9 wherein the bias value is 44.

1 11. The apparatus of claim 10 wherein the correlation result is
2 represented by 6-bit including a sign bit.

1 12. The apparatus of claim 1 wherein $N = 22$ and $K = 12$.

1 13. The apparatus of claim 1 wherein the first clock frequency is two
2 times a coarse/acquisition chip rate of the GPS.

1 14. The apparatus of claim 1 wherein the second clock frequency is
2 equal to the first clock frequency divided by N.

1 15. The apparatus of claim 1 wherein the third clock frequency is equal
2 to the first clock frequency.

1 16. A method comprising:

2 circularly shifting a first data sample of N data samples in a circular shift
3 register into a data position at a first clock frequency, the N data samples
4 corresponding to signal received from one of K satellites in a global positioning
5 system (GPS), the N data samples being loaded into the circular shift register at a
6 second clock frequency;

K, N defined

7 storing K code sequences in K storage elements, respectively, each of the
8 K code sequences having N code samples and including a first code sample being
9 written at a code position corresponding to the data position at a third clock
10 frequency, the K storage elements corresponding to the K satellites; and

11 storing the N code samples loaded from one of the K storage elements in a
12 code register at a fourth clock frequency, the fourth clock frequency being K times
13 faster than the first clock frequency.

1 17. The method of claim 16 further comprising:

2 writing the K first code samples to the K storage elements, respectively, at
3 the K code positions synchronously with the shifted first data sample.

1 18. The method of claim 16 further comprising:

2 computing a correlation result from the N data samples and the N code
3 samples.

1 19. The method of claim 16 wherein each of the K storage elements is
2 one of a plurality of flip-flops, a register, a row in a random access memory
3 (RAM).

1 20. The method of claim 17 wherein writing the K first code samples
2 comprises:

3 enabling writing the K first code samples to the K code positions
4 synchronously with the shifted first data sample.

1 21. The method of claim 18 wherein computing the correlation result
2 comprises:

3 mapping the N data samples and the corresponding N code samples into a
4 plurality of mapper out puts;

5 adding the plurality of mapper outputs to generate a result sum; and

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6         subtracting a bias value from the result sum to generate the correlation
7     result.

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1 22. The method of claim 21 wherein each of the N code samples is a
2 pseudo random noise (PN) code being represented by a one-bit value.

1 23. The method of claim 22 wherein each of the N data samples is a
2 two-bit with value of one of 01, 10, and 11.

1 24. The method of claim 23 wherein each of the mapper outputs is
2 two-bit with value of one of 01, 10, and 11.

1 25. The method of claim 24 wherein the bias value is 44.

1 26. The method of claim 25 wherein the correlation result is
2 represented by 6-bit including a sign bit.

1 27. The method of claim 16 wherein $N = 22$ and $K = 12$.

1 28. The method of claim 16 wherein the first clock frequency is two
2 times a coarse/acquisition chip rate of the GPS.

1 29. The method of claim 16 wherein the second clock frequency is
2 equal to the first clock frequency divided by N.

1 30. The method of claim 16 wherein the third clock frequency is equal
2 to the first clock frequency.

1 31. A receiver comprising:

2 a mixer to generate mixer output samples from a signal received from one

3 of K satellites in a global positioning system (GPS), the mixer output samples

4 including in-phase and quadrature components; K

5 a pseudo-random noise (PN) code generator to generate PN code

6 sequences; and

7 a de-spreader circuit coupled to the mixer and the PN code generator to de-

8 spread the mixer output samples, the de-spreader circuit comprising:

9 a circular shift register having N data samples of the mixer output

10 samples to circularly shift a first data sample of the N data samples

11 into a data position at a first clock frequency, the N data samples

12 corresponding to the signal, the N data samples being loaded into,

13 the circular shift register at a second clock frequency, N

14 K storage elements to store K code sequences, respectively, from

15 the PN code generator, each of the K code sequences having N

16 code samples and including a first code sample being written at a

17 code position corresponding to the data position at a third clock

18 frequency, the K storage elements corresponding to the K satellites,

19 and

20 a code register to store the N code samples loaded from one of the

21 K storage elements at a fourth clock frequency, the fourth clock

22 frequency being K times faster than the first clock frequency.

1 32. The receiver of claim 31 further comprising:
2 a write circuit coupled to the K storage elements to write the K first code
3 samples to the K storage elements, respectively, at the K code positions
4 synchronously with the shifted first data sample.

1 33. The receiver of claim 31 further comprising:
2 a correlator circuit coupled to the circular shift register and the code
3 register to compute a correlation result from the N data samples and the N code
4 samples.

1 34. The receiver of claim 31 wherein each of the K storage elements is
2 one of a plurality of flip-flops, a register, a row in a random access memory
3 (RAM).

1 35. The receiver of claim 32 wherein the write circuit comprises:
2 a plurality of decoders coupled to the K storage elements to enable writing
3 the K first code samples to the K code positions synchronously with the shifted
4 first data sample.

1 36. The receiver of claim 33 wherein the correlator circuit comprises:

2 a mapper to map the N data samples and the corresponding N code
3 samples into a plurality of mapper out puts;
4 an adder to add the plurality of mapper outputs to generate a result sum;
5 and
6 a subtractor to subtract a bias value from the result sum to generate the
7 correlation result.

1 37. The receiver of claim 36 wherein each of the N code samples is a
2 pseudo random noise (PN) code being represented by a one-bit value.

1 38. The receiver of claim 37 wherein each of the N data samples is a
2 two-bit with value of one of 01, 10, and 11.

1 39. The receiver of claim 38 wherein each of the mapper outputs is
2 two-bit with value of one of 01, 10, and 11.

1 40. The receiver of claim 39 wherein the bias value is 44.

1 41. The receiver of claim 40 wherein the correlation result is
2 represented by 6-bit including a sign bit.

1 42. The receiver of claim 41 wherein $N = 22$ and $K = 12$.

